REMARKS

Claims 1-2, 4-5 and 7-15 are pending in this application. By this Amendment, claims 1, 4, 7 and 9 are amended and claims 3 and 6 are canceled without prejudice or disclaimer to the subject matter therein. Further, claims 10-15 are added. Support for the amendments to claims 1, 4, 7, 9 and additional claims 14 and 15, may be found at least at originally filed claims 1 and 3, and paragraphs [0096]-[0098] of the published application. Support for claims 10 and 12 may be found at least at paragraph [0031] of the published application. No new matter is added by the above amendment. In view of at least the following, reconsideration and allowance are respectfully requested.

I. Interview Summary

Applicants appreciate the courtesies shown to Applicants' representatives by Examiner Woldermariam in the November 12, 2008 personal interview. Applicants' separate record of the substance of the interview is incorporated into the following remarks.

II. Claim Rejection under 35 U.S.C. §112

The Office Action rejects claims 1, 4, 7 and 9 under 35 U.S.C. §112, second paragraph. This rejection is respectfully traversed.

By this Amendment, claims 1, 4, 7 and 9 are amended to clarify that the processing order may include a plurality of processes to be executed either (i) serially, (ii) parallel, and (iii) both serially and in parallel. Applicants respectfully submit that claims 1, 4, 7 and 9 are definite and thus comport with the requirements set forth under 35 U.S.C. §112, second paragraph.

Accordingly, withdrawal of the rejection is respectfully requested.

III. Claim Rejection under 35 U.S.C. §103

The Office Action rejects claims 1-9 under 35 U.S.C. §103(a) over U.S. Patent Application Publication No. 2003/0142126 (Estrada) in view of Japanese Publication No. 2001-216452 (Kenichi). This rejection is respectfully traversed.

Independent claim 1 recites, in part, "an interpreting unit that determines whether the instruction data includes instruction which instructs to execute a plurality of parallel-executable processes in serial; [and] a rewriting unit that rewrites the instruction data to instruct to execute the plurality of parallel-executable processes in parallel under the condition that the interpreting unit determines that instruction data includes instruction which instructs to execute a plurality of parallel-executable processes in serial."

Independent claim 4 recites, in part, "determining whether the instruction data includes instruction which instructs to execute a plurality of parallel-executable processes in serial; [and] rewriting the instruction data to instruct to execute the plurality of parallel-executable processes in parallel under the condition that the instruction data is determined to include instruction which instructs to execute a plurality of parallel-executable processes in serial."

Independent claim 7 recites, in part, "an interpreting unit that determines whether the instruction data includes instruction which instructs to execute a plurality of parallel-executable processes in serial; [and] a rewriting unit that rewrites the instruction data to instruct to execute the plurality of parallel-executable processes in parallel under the condition that the interpreting unit determines that instruction data includes instruction which instructs to execute a plurality of parallel-executable processes in serial."

Independent claim 9 recites, in part, "determining whether the instruction data includes instruction which instructs to execute a plurality of parallel-executable processes in serial; [and] rewriting the instruction data to instruct to execute the plurality of parallel-executable processes

in parallel under the condition that the instruction data is determined to include instruction which instructs to execute a plurality of parallel-executable processes in serial."

Estrada and Kenichi, individually or in combination, do not teach, disclose or suggest rewriting instruction data to execute a plurality of parallel-executable processes in parallel under the condition that the instruction data is determined to include instruction which instructs to execute the plurality of parallel processes in serial. Therefore, Estrada and Kenichi, either individually or in combination, do not anticipate or render obvious the subject matter recited in claims 1, 4, 7 and 9.

Claims 2, 5 and 8 variously depend from claims 1, 4, and 7. Because the applied references, in any combination, fail to render the subject matter of independent claims 1, 7, and 9 obvious, dependent claims 2, 5 and 8 are patentable for at least the reasons that claims 1, 4 and 7 are patentable, as well as for the additional features they recite.

Accordingly, withdrawal of the rejection is respectfully requested.

IV. New Claims

By this Amendment, claims 10-15 are added. Claims 10-13 and 15 variously depend from claims 1 and 4. Thus, claims 10-13 and 15 are allowable for the same reasons that claims 1 and 4 are allowable as well as for the additional features they recite.

The applied references, in any combination, fail to disclose rewriting the instruction data to instruct to execute the plurality of parallel-executable processes in parallel under the condition that the instruction data is determined to include instruction which instructs to execute a plurality of parallel-executable processes in serial. Thus, the applied references, either individually or in combination, fail to anticipate or render obvious the subject matter recited in independent claim 14.

Accordingly, allowance of the claims is respectfully requested.

V. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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JAO:DQS/amt

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